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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,085	11/27/2001	Yoshiyuki Uchinono	11411/002001	9568

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ROSENTHAL & OSHA L.L.P.
1221 MCKINNEY AVENUE
SUITE 2800
HOUSTON, TX 77010

EXAMINER

DINH, TUAN T

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 07/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary**Application No.**

09/995,085

Applicant(s)

UCHINONO ET AL.

Examiner

Tuan T Dinh

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 May 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: Attached Disclosed papers

DETAILED ACTION

The request filed on 05/29/03 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/995,085 is acceptable and a RCE has been established. An action on the RCE follows.

Claim Objections

Claims 3, 5, and 7 are objected to because of the following informalities:

Claim 3, line 1, please, delete "the"

Claims 5 and 7, please, change "circuit patter" to --circuit pattern--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nellissen (U. S. Patent 5,937,493).

As to claim 1, Nellissen discloses a multilayer circuit board as shown in figures 1-9 comprising:

a substrate (9, column 6, line 27) having first and second surfaces (100, 200-figures 4-6, see attached paper) extending from an end and the first surface at a required angle relative to the first surface;

a multilayer circuit (13, 15, 19) formed on the first surface of said substrate and composed of a plurality of circuit layers (see figures 6-9), each of which is provided with a conductive layer (13, column 6, lines 29-34) having a required circuit pattern and an insulation layer (15, column 6, lines 43-44) formed on said conductive layer;

a second conductive layer (19, column 6, line 52) formed on the second surface (200, see attached paper) of said substrate by which said conductive layer of one of said circuit layers is electrically to said conductive layer of another one of said circuit layers (13, 15, and 19).

The limitation "an insulation layer formed on said conductive layer by firm formation" has been consider. However, the presence of process limitation in product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to that product. In re Stephens 145 USPQ 656 (CCPA 1965).

Nellissen also discloses method of vapor deposition and laser ablation deposition techniques to provide pattern masks onto the substrate of the multilayer circuit board (column 2, lines 51-57, column 3, lines 34-51); wherein the second surface (200) of said substrate (9) includes a side surface (200') of a projection (5) on the first surface (100), see attaching drawing papers.

As to claim 6, Nellissen discloses a multilayer circuit board as shown in figures 1-15 wherein said second conductive layer (19) is a plurality of second conductive layers

(23) to obtain plural layer-to-layer connections of said multilayer circuit, each of second conductive layers (23) is separated from an adjacent second conductive layer (19) in the thickness direction by a second insulation layer (21).

As to claim 5, Nellissen discloses a multilayer circuit board as shown in figures 1-15 comprising:

- a substrate (9, column 6, line 27) having first and second surfaces (100, 200-figures 4-6, see attached paper) extending from an end and the first surface at a required angle relative to the first surface;

- a multiplayer circuit (13, 15, 19) formed on the first surface of said substrate and composed of a plurality of circuit layers (see figures 6-9), each of which is provided with a conductive layer (13, column 6, lines 29-34) having a required circuit pattern and an insulation layer (15, column 6, lines 43-44) formed on said conductive layer;

- a second conductive layer (19, column 6, line 52) formed on the second surface (200, see attached paper) of said substrate by which said conductive layer of one of said circuit layers is electrically to said conductive layer of another one of said circuit layers (13, 15, and 19);

wherein said multilayer circuit has an aperture (7-figure 2, column 6, lines 24-25), through which a part of the first surface is exposed, and an electronic device (37, column 7, lines 45-50)) is mounted in a concave formed in the exposed first surface, and an electrical connection between said multilayer circuit and said electronic device is made by a third conductive layer (29, column 7, line 8) formed on an inner surface of said concave.

The limitation "an insulation layer formed on said conductive layer by firm formation" has been considered. However, the presence of process limitation in product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to that product. In re Stephens 145 USPQ 656 (CCPA 1965).

Nellissen also discloses method of vapor deposition and laser ablation deposition techniques to provide pattern masks onto the substrate of the multilayer circuit board (column 2, lines 51-57, column 3, lines 34-51); wherein the second surface (200) of said substrate (9) includes a side surface of a projection (5) on the first surface (100).

As to claim 7, Nellissen discloses a multilayer circuit board as shown in figures 1-15 comprising:

- a substrate (9, column 6, line 27) having first and second surfaces (100, 200-figures 4-6, see attached paper) extending from an end and the first surface at a required angle relative to the first surface;

- a multilayer circuit (13, 15, 19) formed on the first surface of said substrate and composed of a plurality of circuit layers (see figures 6-9), each of which is provided with a conductive layer (13, column 6, lines 29-34) having a required circuit pattern and an insulation layer (15, column 6, lines 43-44) formed on said conductive layer;

- a second conductive layer (19, column 6, line 52) formed on the second surface (200, see attached paper) of said substrate by which said conductive layer of one of said circuit layers is electrically to said conductive layer of another one of said circuit layers (13, 15, and 19);

wherein said substrate (9) has a third surface (300) extending at a different level from the first surface and a fourth surface (400) extending from the other end of the first surface to an end of the third surface (see figure 2 of the attaching drawing papers), and said multilayer circuit is formed on the first, third and fourth surfaces of said substrate, and said second conductive layer is formed on a side surface of a projection on the first surface to make the layer-to-layer connection of said multilayer circuit.

The limitation "an insulation layer formed on said conductive layer by firm formation" has been consider. However, the presence of process limitation in product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to that product. In re Stephens 145 USPQ 656 (CCPA 1965).

Nellissen also discloses method of vapor deposition and laser ablation deposition techniques to provide pattern masks onto the substrate of the multiplayer circuit board (column 2, lines 51-57, column 3, lines 34-51); wherein the second surface (200) of said substrate (9) includes a side surface of a projection (5) on the first surface (100).

3. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nellisen (U. S. Patent 5,937,493) in view of Roberts (U. S. Patent 5,584,120).

Nellisen does not disclose the first surface is a top surface of said substrate, and the second surface is a side surface of said substrate, and the required angle between the first and second surfaces is an obtuse angle.

Roberts shows a multiplayer circuit board as shown in figures 1-10 comprising a substrate (1) having a first surface (16), which is a top surface of the substrate (1) and a second surface (15), which is a side surface of the substrate, the require angle between the first and second surfaces is an obtuse angle.

It would have been obvious to one having skill in the art at the time the invention was made to a first surface on top of a second surface and having an angle, which is obtuse angle as taught by Roberts to employ the multiplayer circuit board of Nellisen in order to provide a reliability and flexibility of a circuit design for the multiplayer circuit board.

Response to Arguments

4. Applicant's arguments with respect to claims 1, and 3-7 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues:

(a) Nellissen does not teach "a second conductive layer...on the first surface"

(b) Nellissen does not teach "a part of the first surface is exposed, and an electronic device mounted in a concave formed in the exposed first surface"

Examiner disagrees.

Response to argument (a), Nellissen clearly shows a conductive layer (19) formed on a second surface (200) of a substrate (9), see figures 2-6, and also, Nellissen discloses the second surface including a side surface (200') of a projection (5) on a first surface (100).

Response to argument (b), Nellissen clearly shows a part of the first surface is exposed, which is one of a stackable of layers (13, 15,, 19, 23, ad 25), and an electronic device (37) mounted in a concavity (an opening 7 of the substrate 9) formed in the exposed first surface (100).


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD
June 25, 2003.



DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800